ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes first and second select transistors arranged on both sides of a shared-scheme sense amplifier and connected to a bit line, and first and second memory cell arrays connected to the bit line via the first and second select transistors, respectively, the first and second memory cell arrays each including a plurality of memory cells each having a cell transistor and a ferroelectric capacitor. The device further includes a setting circuit which controls the first and second select transistors, thereby setting the first and second memory cell arrays in an operative state at the same time, and a control circuit which performs a test at the same time for the first and second memory cell arrays, which are set in the operative state at the same time by the setting circuit.